Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1 (Previously Presented): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode;

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling

phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode by a film located above said first and second control gate electrodes, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 2 (Original): A semiconductor memory according to claim 1, wherein materials of said floating gate electrode and a channel region between said pair of impurity doped regions are selected so that a Fermi level of said floating gate electrode is in a forbidden band of the channel region when an external voltage is not applied between the channel region and said first control gate electrode.

Claims 3 – 11 (Canceled).

Claim 12 (Previously Presented): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness of at most 3nm;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit theretbrough by a direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode;

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode by a film located above said first and second control gate electrodes, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 13 (Currently Amended): A semiconductor memory according to claim 12, wherein said tunneling insulating film has a thickness of at least 2 [[mm]] nm.

Claim 14 (Previously Presented): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode;

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode by a film located above said first and second control gate electrodes, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein a surface layer of said semiconductor substrate under said first control gate electrode has a conductivity opposite to that of said impurity doped regions, and

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 15 (Previously Presented): A semiconductor memory according to claim 1, wherein the top surfaces of the impurity doped regions are covered with a metal silicide film, and

the film located above the first and second control gate electrodes is made of the same material as the metal silicide film.

Claim 16 (Canceled).